# Trends in HPC and HPEC Convergence

Richard Games rg@mitre.org



maintaining the data needed, and of including suggestions for reducing	llection of information is estimated to completing and reviewing the collect this burden, to Washington Headqu uld be aware that notwithstanding ar OMB control number.	ion of information. Send comments arters Services, Directorate for Information	regarding this burden estimate or mation Operations and Reports	or any other aspect of th , 1215 Jefferson Davis I	is collection of information, Highway, Suite 1204, Arlington	
1. REPORT DATE 21 MAY 2003	2. REPORT TYPE <b>N/A</b>			3. DATES COVERED		
4. TITLE AND SUBTITLE			5a. CONTRACT NUMBER			
Trends in HPC and HPEC Convergence				5b. GRANT NUMBER		
				5c. PROGRAM ELEMENT NUMBER		
6. AUTHOR(S)				5d. PROJECT NUMBER		
				5e. TASK NUMBER		
				5f. WORK UNIT NUMBER		
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)  The MITRE Corporation				8. PERFORMING ORGANIZATION REPORT NUMBER		
9. SPONSORING/MONITO		10. SPONSOR/MONITOR'S ACRONYM(S)				
				11. SPONSOR/MONITOR'S REPORT NUMBER(S)		
12. DISTRIBUTION/AVAILABILITY STATEMENT  Approved for public release, distribution unlimited						
13. SUPPLEMENTARY NOTES  Also see ADM001473, The original document contains color images.						
14. ABSTRACT						
15. SUBJECT TERMS						
16. SECURITY CLASSIFIC	17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON			
a. REPORT unclassified	b. ABSTRACT <b>unclassified</b>	c. THIS PAGE unclassified	UU	18	ALSI UNSIBLE FERSUN	

**Report Documentation Page** 

Form Approved OMB No. 0704-0188

 Over the last 10 years R&D investments have made high performance embedded computing for national security applications more like mainstream high performance computing

 Over the next 10 years R&D investments will make mainstream high performance computing for national security applications more like high performance embedded computing



- Over the last 10 years R&D investments have made high performance embedded computing for national security applications more like mainstream high performance computing
  - DARPA Touchstone
  - DARPA Embedded Systems
  - OSD High Performance Embedded Computing Software Initiative
- Over the next 10 years R&D investments will make mainstream high performance computing for national security applications more like high performance embedded computing
  - DARPA Adaptive Computing
  - DARPA Data Intensive Systems
  - DARPA Polymorphic Computing Architectures
  - DARPA High Productivity Computing Systems



- Over the last 10 years R&D investments have made high performance embedded computing for national security applications more like mainstream high performance computing
  - DARPA Touchstone
  - DARPA Embeddable Systems
  - OSD High Performance Embedded Computing Software Initiative
- Over the next 10 years R&D investments will make mainstream high performance computing for national security applications more like high performance embedded computing
  - DARPA Adaptive Computing
  - DARPA Data Intensive Systems
  - DARPA Polymorphic Computing Architectures
  - DARPA High Productivity Computing Systems



## **HPEC Software Initiative**



### **Program Goals**

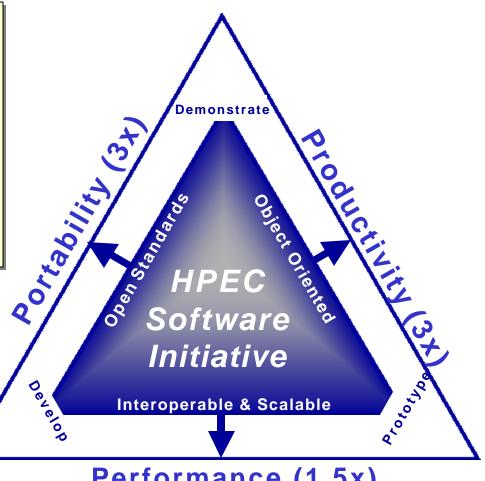
- Develop and integrate software technologies for embedded parallel systems to address portability, productivity, and performance
- Engage acquisition community to promote technology insertion
- **Deliver quantifiable benefits**

**Portability: reduction in lines-of** code to change port/scale to new system

**Productivity: reduction in overall** 

lines-of-code

**Performance:**computation and communication benchmarks



Performance (1.5x)





## Common Imagery Processor Experiment Overview

## Software Middleware Standards

MPI VSIPL DRI Sensor Feed - I/O Processor Each server or multicomputer forms an independent signal processor. The I/O server round robins data to each signal processor to meet throughput









### **Shared Memory Servers**

**Distributed Memory Multicomputers** 

Distributed memory CIP software would allow insertion of embedded multicomputer or commodity clusters as a signal processor in CIP system



## **HPEC-SI Middleware**

### **Development**

### VSIPL++

### **MAPPING** (data parallelism)

- -Early binding (computations)
- -Compatibility (backward/forward)
- -Local Knowledge (accessing local data)
- -Extensibility (adding new functions)
- -Remote Procedure Calls (CORBA)
- -C++ Compiler Support
- -Test Suite
- -Adoption Incentives (vendor, integrator)

### **Applied Research**

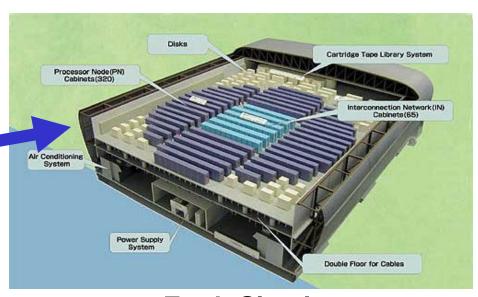
### Parallel VSIPL++

- -MAPPING (task/pipeline parallel)
- -Reconfiguration (for fault tolerance)
- -Threads
- -Reliability/Availability
- -Data Permutation (DRI functionality)
- -Tools (profiles, timers, ...)
- -Quality of Service



## From the Small to the Big





### **Earth Simulator**

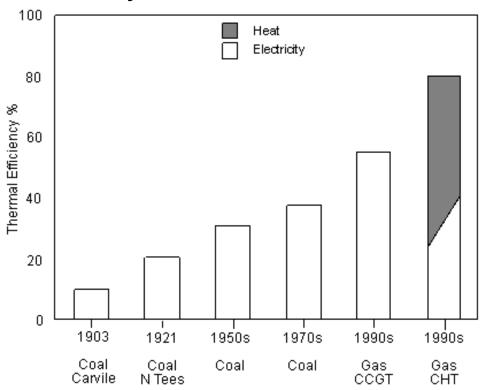
Earth Simulator pictures from www.es.jamstec.go.jp/esc/eng JSTARS pictures courtesy of Northrop Grumman



## **Efficiency: The Big Picture**

Losses accumulate from the point of electricity generation, through distribution, and *finally during utilization by the end user* 

### **Efficiency of Electrical Power Generation**



One Ton of Coal Generated

<u>Year</u>	<b>Energy</b>				
1891	150 kWh				
1914	550 kWh				
1920	630 kWh				
1939	1566 kWh				
2002	3000 kWh				
<b>Electricity distribution</b>					
efficiency: 92%					

ASCI Q: 24 - 30 Tflop/s (peak) 3 megawatts to run plus 2 megawatts to cool (energy for 5000 homes)

Computing efficiency
Gflop/s
Percent peak
Gflop/s/Watt

www.electricity.org.uk/uk\_inds/environ/env\_19.html www.parcon.uci.edu/paper/energy.htm

**MITRE** 



## High Productivity Computing Systems

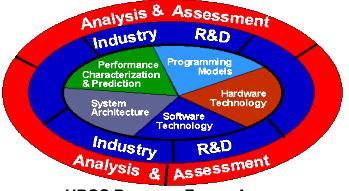


### Goals:

 Provide a new generation of economically viable high productivity computing systems for the national security and industrial user community (2007 – 2010)

### Impact:

- Performance (efficiency): critical national security applications by a factor of 10X to 40X
- Productivity (time-to-solution)
- Portability (transparency): insulate research and operational application software from system
- Robustness (reliability): apply all known techniques to protect against outside attacks, hardware faults, & programming errors

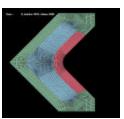


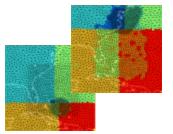
**HPCS Program Focus Areas** 













### **Applications:**

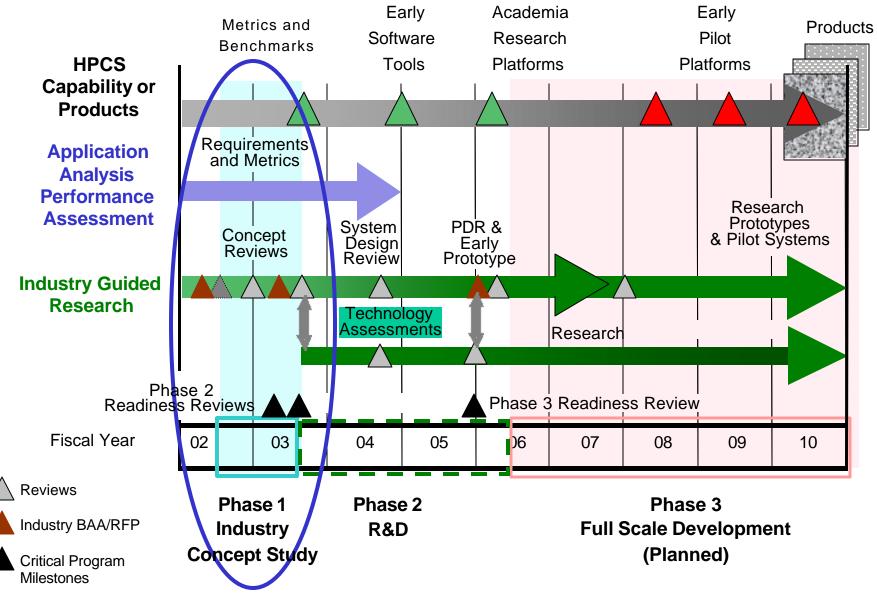
 Intelligence/surveillance, reconnaissance, cryptanalysis, weapons analysis, airborne contaminant modeling and biotechnology

Fill the Critical Technology and Capability Gap
Today (late 80's HPC technology).....to.....Future (Quantum/Bio Computing)

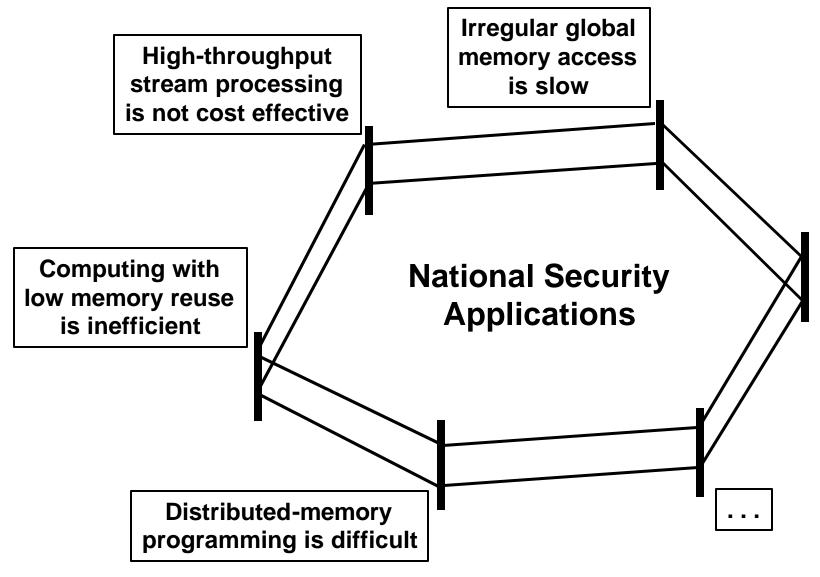


## **HPCS Program Phases 1-3**





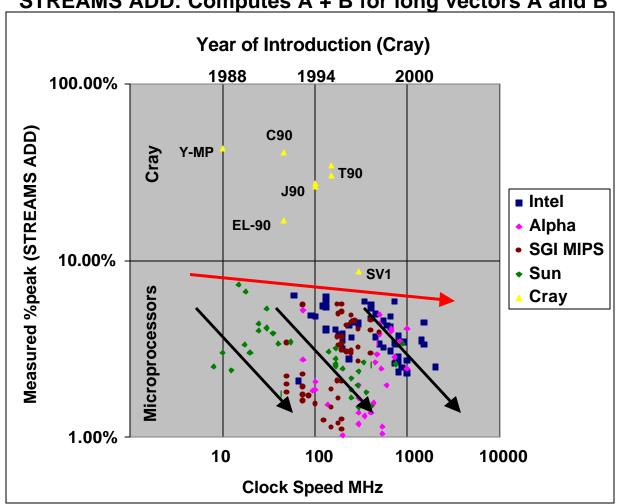
## **Bounding the HPCS Challenges**





## Why applications with limited memory reuse perform inefficiently today

STREAMS ADD: Computes A + B for long vectors A and B

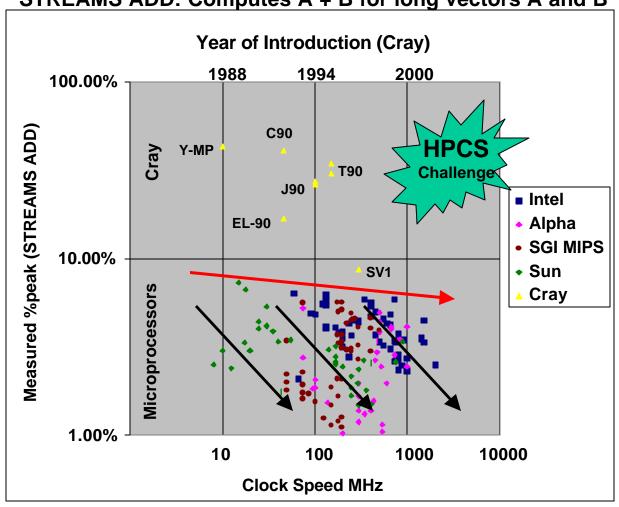


- New microprocessor generations "reset" performance to around 6% of peak
- Performance degrades to 1% 3% of peak as clock speed increases



## Why applications with limited memory reuse perform inefficiently today

STREAMS ADD: Computes A + B for long vectors A and B



- New microprocessor generations "reset" performance to around 6% of peak
- Performance degrades to 1% 3% of peak as clock speed increases



## Long FFTs are Inefficient

#### CacheBench

Direct correlation between memory bandwidth from various levels of the memory hierarchy and the performance of real applications

> 100.00 90.00 80.00

> > 70.00

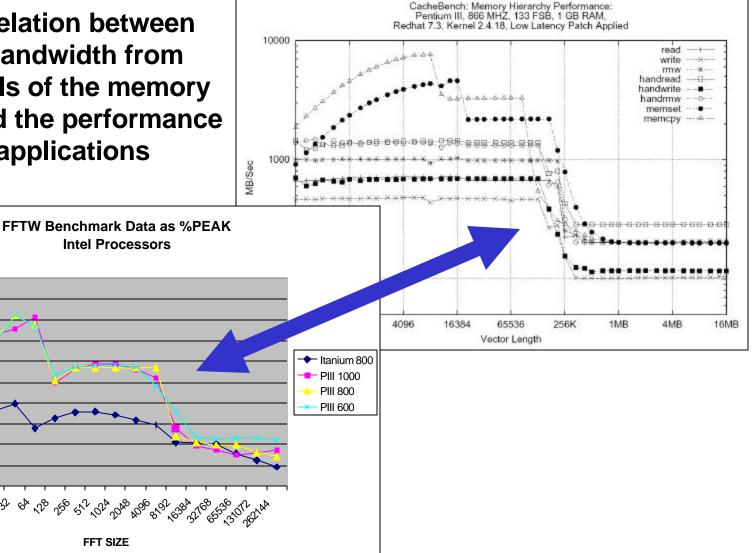
60.00

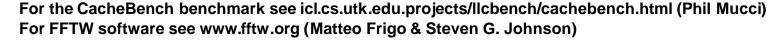
50.00

40.00

30.00 20.00 10.00 0.00 Intel Processors

**FFT SIZE** 



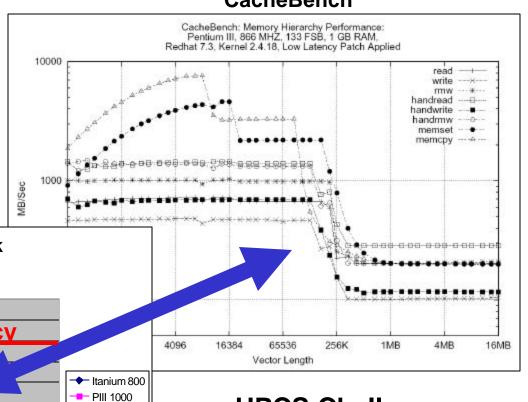




## Long FFTs are Inefficient

#### CacheBench

Direct correlation between memory bandwidth from various levels of the memory hierarchy and the performance of real applications



### FFTW Benchmark Data as %PEAK Intel Processors 100.00 90.00 **HPCS Efficiency** 80.00 70.00 60.00 50.00 PIII 800 40.00 PIII 600 30.00 20.00 10.00 0.00 **FFT SIZE**

HPCS Challenge
Cost effective signal
processing in software
for high throughput
streaming applications

For the CacheBench benchmark see icl.cs.utk.edu.projects/llcbench/cachebench.html (Phil Mucci) For FFTW software see www.fftw.org (Matteo Frigo & Steven G. Johnson)



## **Value Proposition: Metrics**

### **Producer**

- Sells computers
- Sells support
- Profit
- Market share
- Stockholder's equity
- Reputation
- Peak rates
- Customer satisfaction
- Deliver solutions
- Novel technology
- ...

### **Consumer**

- Has national security mission
- Needs a computer to process data or calculate answers
- In time--time to solution
- Fits (size, weight, power)
- Easy to program--idea to sol'n
- Affordable--life-cycle, facilities and support costs
- Efficient--sustained rates
- Reliable
- Evolvable
- . . .



- Over the last 10 years R&D investments have made high performance embedded computing for national security applications more like mainstream high performance computing
  - Looking for good HPEC-SI demonstrations
- Over the next 10 years R&D investments will make mainstream high performance computing for national security applications more like high performance embedded computing
  - Looking for good HPCS challenge problems

Richard Games, rg@mitre.org

